

TITLE

METHOD FOR ADAPTIVE CONTROL OF DRAM
REFRESH INTERVAL

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates in general to a technology for controlling the refresh interval of dynamic random access memory (DRAM), and more particularly to a method and apparatus for DRAM self-testing at startup.

10 Description of the Related Art

DRAM, the most commonly used solid state access memory chip provides many advantages, such as high density, low cost, and high operating speed among others. DRAM stores memory data by electric charge, however, and the electric charge gradually lost
15 over time by the reverse bias voltage leakage current of the PN junction of the NMOS transistor in the DRAM memory cell. Hence, the DRAM chip must be continuously updated, even in stand-by mode, to prevent data loss over time. The process of updating DRAM memory data is known as a refresh and the time elapsed
20 between refresh processes is known as the refresh interval. A high frequency, or shorter, refresh interval is inefficient as it consumes excessive power.

Power management in primarily battery powered devices such as PDAs and cell phones, is particularly important as power must
25 be consumed as conservatively as possible to prolong battery life.

Therefore, reducing power consumption has become the most important issue in DRAM research, especially regarding the refresh interval.

SUMMARY OF THE INVENTION

5 Accordingly, an object of the present invention is to provide an appropriate refresh interval for reducing the power consumption.

10 The present invention provides a method for determining an appropriate refresh interval comprising, detecting startup, providing a clock pulse as a refresh interval, DRAM self-testing of a plurality of memory cells with the provided refresh interval, modifying the refresh interval and repeating the above steps to find the longest refresh interval as determined by the DRAM self-testing procedure, and using the determined
15 appropriate refresh interval to refresh the DRAM.

 Additionally, to prevent data loss and reduce power consumption in stand-by mode, the refresh interval must frequent enough to sufficiently refresh the DRAM, while still offering reduced power consumption.

20 Accordingly, the DRAM self-test at startup of the present invention enables use of a refresh interval appropriate for maintaining data and reducing power consumption.

 A detailed description is given in the following with reference to the accompanying drawings.

25 BRIEF DESCRIPTION OF THE DRAWINGS

 The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

 Fig. 1 is a flow chart diagram of the present invention;

Fig. 2 is a circuit diagram of a ring-type oscillator of the present invention;

Fig. 3 is a circuit diagram of a phase inverter of Fig. 2; and

5 Fig. 4 is a schematic diagram of the control voltage circuit shown in Fig. 3;

DETAILED DESCRIPTION OF THE INVENTION

The object of the present invention is to determine an appropriate refresh interval by DRAM self-testing at startup.

10 Fig. 1 is flowchart diagram of the present invention. When startup 5 is detected a refresh interval 10 is provided for DRAM for self-testing. The self-testing procedure continues for a plurality of memory cells 12 until the longest refresh interval 22 is determined. Finally, the DRAM 26 is refreshed using the
15 longest refresh interval as determined by self-testing.

The object of the self-testing procedure 12 is to prevent data loss by using the appropriate refresh interval 10. Thus, during the self-testing procedure 12, an original test code is first written to a plurality of the memory cells 14. The memory
20 cells are then refreshed using the provided refresh interval. The saved test code is then read from the memory cell 18, and finally, the saved test code is compared with the original test code 20. An equal result obtained in step 20 indicates that the present refresh interval is sufficient to prevent data loss. An
25 unequal result obtained in step 20 indicates that the present refresh interval is too long to sufficiently prevent data loss.

Additionally, if after the first loop of the self-testing procedure to find the longest refresh interval, the result of step 20 is equal the current refresh interval is increased and

the procedure returns to step 12 until the result of step 20 is unequal.

In contrast, if after the first loop of the self-testing procedure to find the longest refresh interval, the result of
5 step 20 is unequal the current refresh interval is decreased and the procedure returns to step 12 until the result of step 20 is equal.

Hence, a refresh interval capable of both preventing data loss and reducing power consumption can be determined by the
10 self-testing method 10 described in the following.

The refresh interval may be determined, however, from testing only a sample of the total number of memory cells, which still leaves a measure of uncertainty regarding effectiveness. Thus, it is necessary to determine a refresh interval capable
15 of attaining the goals of data retention and reduced power consumption.

Thus, the appropriate refresh interval is determined as the longest refresh interval plus a specific variable, to prevent refresh failure in other memory cells while maintaining improved
20 performance.

Finally, by using the appropriate refresh interval refresh DRAM during normal operation prevents data loss and reduced power consumed by the refresh interval.

The length and the content of the original test code can
25 be designed as a DRAM array structure or be chosen at random.

Referring to Fig. 2, a ring-type oscillator 32 of the present invention is shown, wherein the ring-type oscillator 32 comprises an odd number of phase inverter 30 connected in series, and the output port of the final one end is connected to the input

port of the first phase inverter 30 to act as a ring-type oscillator 32.

Fig. 3 is a circuit diagram of a phase inverter 30 of Fig. 2, wherein the driving current of the phase inverter 30 is controlled by a potential V_0 . In fig. 2, the potential V_0 controls the discharged current of phase inverter 30 to modify the oscillatory period of the ring-type oscillator 32. For example, discharged current can be increased by elevating the potential V_0 , thus decreasing oscillatory period T .

Fig. 4 is a schematic diagram of the control voltage circuit shown in Fig. 3, wherein the counter 34 is controlled by an up/down control signal to output a control value. After receiving the control value, a digital-to-analog converter (D/A converter) 36 outputs the potential V_0 . Thus, as shown in fig. 1, the up/down control signal value is determined by step 22. For example, to increase the potential V_0 and reduce the oscillatory period of the ring-type oscillator 32 when the refresh interval is too long to maintain data in the memory cell, the value of counter 34 is increased. Conversely, the value of counter 34 is reduced to increase the oscillatory period until the appropriate refresh interval is determined.

Hence, by using the present values of counter 34, the system can determine the appropriate refresh interval after determining the longest refresh interval.

Therefore, comparatively, the appropriate refresh interval can be determined by the method of the present invention, and ameliorates the disadvantages of the prior art.

While the invention has been described by way of example and in terms of the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments.

On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation to encompass all such
5 modifications and similar arrangements.